CLAIMS

Please cancel Claims 1-11, amend Claims 14-15 and 20, and add Claims 21-40 as shown in the Listing of the Claims that follows. This listing replaces all prior versions and listings of claims associated with the present Application.

LISTING OF THE CLAIMS

1-11. (canceled)

12. (original) A method of improving the performance of address translation in a translation lookaside buffer comprising using a bit obtained from a virtual page number to consolidate even and odd page frame numbers into a single page frame number field of said translation lookaside buffer.

13. (original) The method of Claim 12 wherein said bit corresponds to the least significant bit of said virtual page number.

14. (currently amended) The method of Claim 12 wherein said address translation of said translation look aside buffer is performed by way of using ~~an existing~~ control processor instruction set.

15. (currently amended) The method of Claim 12 wherein said consolidating even and odd page frame numbers into saida single page frame number field implements a translation lookaside buffer of reduced size.

16. (original) A system to provide effective virtual to physical memory address translation comprising a buffer that uses a single page frame number field for storing odd/even page frame numbers.

17. (original) The system of Claim 16 wherein said buffer comprises a translation lookaside buffer of reduced size.

18. (original) A system to provide virtual to physical memory address translation of a translation lookaside buffer comprising:

a translation lookaside buffer, said translation lookaside buffer using a bit of a virtual page number of a virtual address for reading and writing odd and even page frame numbers using a single page frame number field of said translation lookaside buffer.

19. (original) The system of Claim 18 wherein using a single page frame number field implements a reduced size of said translation lookaside buffer.

20. (currently amended) The system of Claim 19 wherein said virtual to physical memory address translation is performed by way of using ~~existing~~ TLB control processor instructions.

21. (new) A method of implementing a reduced size translation lookaside buffer comprising:

obtaining a bit obtained from a virtual page number of a virtual address;

using said bit to determine which one of two storage registers will be used for writing page frame number data from said one register into said translation lookaside buffer or for reading said page frame number data from a page frame number field of an indexed entry in said translation lookaside buffer;

storing even or odd page frame numbers into a single page frame number field associated with said entry of said translation lookaside buffer by way of using a first storage register of said two storage registers for even page frame numbers and a second storage register of said two storage registers for odd page frame numbers when said writing is performed; and

retrieving said even or odd page frame numbers from a single page frame number field associated with said entry of said translation lookaside buffer by way of using said first or said second storage register when said reading is performed.

22. (new) The method of Claim 21 wherein said bit corresponds to the least significant bit of said virtual page number.

23. (new) The method of Claim 21 wherein said reading and said writing is performed by way of using a translation lookaside buffer (TLB) control processor instruction set.

24. (new) The method of Claim 23 wherein said TLB control processor instruction set comprises a MIPS control processor instruction set.

25. (new) The method of Claim 21 wherein said virtual address comprises 32 bits.

26. (new) The method of Claim 25 wherein said virtual page number is specified by bits [31:12] of said virtual address.

27. (new) The method of Claim 25 wherein said virtual address utilizes a page mask size ranging from 4 kilobytes to 16 megabytes.

28. (new) The method of Claim 27 wherein said page mask size comprises 4 kilobytes.

29. (new) A method of performing a write operation using a translation lookaside buffer comprising:

using a bit of a virtual page number, said virtual page number stored in a data register;

assessing whether a value of said bit of a virtual page number is 0 or 1;

writing a first page frame number stored in a first register to a page frame number field of an indexed entry of said translation lookaside buffer if said value is 0; and

writing a second page frame number stored in a second register to said page frame number field of said indexed entry of said translation lookaside buffer if said value is 1, said indexed entry comprising a single page frame number field used to reduce the size of said translation lookaside buffer.

30. (new) The method of Claim 29 wherein said bit corresponds to the least significant bit of said virtual page number.

31. (new) The method of Claim 29 wherein a control processor is used to verify that said first page frame number and said second page frame number are valid.

32. (new) A method of performing a read operation using a translation lookaside buffer comprising:

using a bit of a virtual page number, said virtual page number stored in virtual page number field of said translation lookaside buffer;

assessing whether a value of a bit of a virtual page number is 0 or 1;

reading a page frame number stored in a page frame number field of an indexed entry of said translation lookaside buffer;

storing said page frame number into a first register if said value is 0; and

storing said page frame number into a second register if said value is 1, said indexed entry comprising a single page frame number field used to reduce the size of said translation lookaside buffer.

33. (new) The method of Claim 32 wherein said bit corresponds to the least significant bit of said virtual page number.

34. (new) A method of probing for a particular virtual page number of an entry in a translation lookaside buffer comprising:

using a virtual page number stored in a first register;

comparing said virtual page number to one or more values stored in one or more virtual page number fields of one or more corresponding entries in said translation lookaside buffer;

generating an identifying number associated with an entry of said one or more entries if a virtual page number field stores a value that is equal to said virtual page number; and

storing said identifying number into a second register.

35. (new) A translation lookaside buffer system comprising:

a translation lookaside buffer;

a first register used for storing a value that indexes an entry in said translation lookaside buffer, said entry comprising a virtual page number field and a single page frame number field;

a second register used for storing a page size of said entry;

a third register used for storing a virtual page number of said entry, said virtual page number comprising a bit;

a fourth register used for storing an even page frame number; and

a fifth register used for storing an odd page frame number, said bit of said virtual page number used to determine whether said even page frame number or said odd page frame number is to be stored in said page frame number field in said translation lookaside buffer when performing a write operation, said bit of said virtual page number stored in said virtual page number field used to determine whether said even page frame number is to be stored in said fourth register or said odd page frame number is to be stored in said fifth register when performing a read operation, wherein use of said single page frame number field reduces the size of said translation lookaside buffer.

36. (new) The method of Claim 35 wherein said read and write operations are performed by way of using a translation lookaside buffer (TLB) control processor instruction set.

37. (new) The method of Claim 36 wherein said TLB control processor instruction set comprises a MIPS control processor instruction set.

38. (new) The method of Claim 35 wherein said virtual page number is defined by a 32 bit virtual address.

39. (new) The method of Claim 38 wherein said virtual page number is specified by bits [31:12] of said 32 bit virtual address.

40. (new) The method of Claim 38 wherein said bit comprises the least significant bit (lsb) of said virtual page number.